WHAT IS CLAIMED

1. For use with a communication system in which a data packet is to be multicast to a plurality of recipients, a method of buffering and controllably supplying said data packet for delivery to multiple ones of a plurality of output ports associated with said recipients comprising the steps of:

(a) storing said data packet in only a single data packet storage location of a data packet buffer;

(b) storing, in a content-addressable memory, a plurality of respectively different address pointer words, each address pointer word containing a respectively different key field that is used to identify one of said plurality of output ports, and an address field that identifies said single data packet storage location of said packet buffer in which said data packet is stored;

(c) coupling a key to said respectively different key fields of said respectively different address pointer words stored in said content addressable memory, so as to access contents of the address field of an address pointer word whose key field matches said key;

(d) reading said data packet from said single data packet storage location of said packet buffer in accordance with said address field contents accessed in step (c); and

(e) coupling said address field contents accessed in step (c) to the address fields of said respectively different address pointer words stored in said content-addressable memory to determine whether said single data packet storage location of said data packet buffer is available to store a new data packet.

2. A method according to claim 1, wherein steps (d) and (e) are conducted during a common memory cycle for said content-addressable memory.

3. A method according to claim 1, wherein step (e) comprises generating a signal representative whether or not said accessed address field contents are contained in the address field of another address pointer word.

4. A method according to claim 1, wherein step (e) comprises generating a signal representative of the availability of said single data packet storage location of said packet buffer to store a new data packet, in accordance with whether or not said address of said data packet single storage location of said packet buffer is contained in another address pointer word stored in said content-addressable memory.

5. A method according to claim 1, wherein said content-addressable memory comprises a data bit storage cell having a data input through which a data bit is written into said data bit storage cell, a data output through which a data bit is read out of said data bit storage cell, and an address input through which said data bit storage cell is selectively accessed, and a data bit comparator coupled to said data bit storage cell and being configured to determine whether the data bit stored in said data bit storage cell matches a reference data bit during a read cycle for said data bit storage cell.

6. A method of interfacing data with a data memory comprising the steps of:

(a) storing said data in said data memory by:

(a1) writing said data into a storage location of said data memory, and

(a2) writing, into one or more respective storage regions of a content-addressable memory, one or more respective address pointer words, each of which includes a respective key field that is used to identify said data, and an address field that identifies the address of said storage location of said data memory;

(b) reading said data from said data memory by:

(b1) coupling a key to key fields of address pointer words stored in storage regions of said content-addressable memory, and accessing said address of said storage location of said data memory from the address field of an address pointer word whose key field contains said key;

(b2) reading said data from said storage location of said data memory in accordance with said address accessed in step (b1); and

(c) coupling said address accessed in step (b1) to said content-addressable memory, to determine whether said address of said storage location of said data memory is contained in another address pointer word stored in said content-addressable memory.

7. A method according to claim 6, wherein steps (b2) and (c) are conducted during a common memory cycle for said content-addressable memory.

8. A method according to claim 6, wherein step (c) comprises selectively making said storage location of said data memory available for storage of new data, in dependence upon whether or not said address of said storage location of said data memory is contained in another address pointer word stored in said content-addressable memory.

9. A method according to claim 6, wherein step (a) comprises writing, into plural storage regions of said content-addressable memory, a plurality of address pointer words, each of which contains a respectively different key field used to identify said data, and said address of said storage location of said data memory.

10. A method according to claim 6, wherein said content-addressable memory comprises a data bit storage cell having a data input through which a data bit is written into said data bit storage cell, a data output through which a data bit is read out of said data bit storage cell, and an address input through which said data bit storage cell is selectively accessed, and a data bit comparator coupled to said data bit storage cell and being configured to determine whether the data bit stored in said data bit storage cell matches a reference data bit during a read cycle for said data bit storage cell.

11. For use with a communication system in which packetized data is to be controllably multicast to a plurality of recipients in accordance with multicast criteria, an output port data distribution architecture for buffering and controllably supplying packetized data for delivery to multiple ones of a plurality of output ports associated with said recipients comprising:

a packet buffer containing a plurality of storage locations that store data packets intended for delivery to one or more of said plurality of output ports;

a content-addressable memory containing a plurality of storage regions that store respectively different address pointer words, each address pointer word containing a respectively different key field that is used to identify a data packet to be delivered to one of said plurality of output ports, and an address field that identifies the address of one of said plurality of storage locations of said packet buffer in which said data packet is stored; and

a packet buffer access controller, which is operative to couple a key to key fields of address pointer words of said plural storage regions of said content-addressable memory, and thereby access contents of the address field of an address pointer word whose key field contains said key, the accessed address field contents being coupled to read out a data packet stored in one of said plurality of storage locations of said packet buffer, said accessed address field contents being coupled to the address fields of address pointer words stored in said content-addressable

memory, and wherein said content-addressable memory is operative to output a signal representative whether said accessed address field contents are contained in the address field of another address pointer word stored in said content-addressable memory.

12. An output port data distribution architecture according to claim 11, wherein said content-addressable memory is operative to output a signal indicating whether or not said storage location of said packet buffer is available for storage of a new data packet, in accordance with whether or not said address of said storage location of said packet buffer is contained in another address pointer word stored in said content-addressable memory.

13. An output port data distribution architecture according to claim 11, wherein said packet buffer access controller is operative to cause a data packet, that is to be multicast to multiple output ports, to be stored in a single storage location of said packet buffer, and to cause multiple address pointer words to be stored in said content-addressable memory, respective ones of said multiple address pointer words containing different key fields for respectively different ones of said multiple output ports, and the same address field that identifies the address of said single data packet storage location of said packet buffer storing said data packet to be multicast.

14. An output port data distribution architecture according to claim 11, wherein said content-addressable memory contains a plurality of storage regions that store respectively different address pointer words, a respective storage region containing a first plurality of content addressable memory cells, the contents of which are associated with a first field of a respective address pointer word that identifies data to be accessed from a storage location in said packet buffer, and a second plurality of content addressable memory cells, the contents of which are associated with a second field of said respective address pointer word that identifies the address of said storage location in said packet buffer.

15. An output port data distribution architecture according to claim 14, wherein respectively different address pointer words stored in multiple ones of said plurality of storage regions of said content addressable memory contain respectively different first fields associated with respectively different ones of multiple instances of accessing said data from said storage location in said packet buffer, and a common second field that identifies the address of said storage location in said packet buffer for each of said multiple instances of accessing said data from said storage location in said packet buffer.

16. An output port data distribution architecture according to claim 15, wherein each of said first plurality of content addressable memory cells is configured to compare contents stored therein with a packet access key associated with data to be accessed from said storage location in said packet buffer, and to selectively read out contents of said second plurality of content addressable memory cells to address said storage location in said packet buffer in accordance with whether or not said packet access key matches said contents of said first plurality of content addressable memory cells.

17. An output port data distribution architecture according to claim 16, wherein each of said plurality of storage regions is further configured to compare contents stored therein with said read out contents of said second plurality of content addressable memory cells to determine whether any other of said plurality of storage regions contains said common second field of said respective address pointer word that identifies said address of said storage location in said packet buffer.

18. An output port data distribution architecture according to claim 17, wherein a respective storage region of said content-addressable memory is configured to output a signal indicating whether or not said storage location of said packet buffer is available for storage of new data, in accordance with whether another of said plurality of storage regions contains said common second field of said respective address pointer word.

19. An output port data distribution architecture according to claim 11, wherein a respective one of said second plurality of content addressable memory cells comprises a data bit storage cell having a data input through which a data bit is written into said data bit storage cell, a data output through which a data bit is read out of said data bit storage cell, and an address input through which said data bit storage cell is selectively accessed, and a data bit comparator coupled to said data bit storage cell and being configured to determine whether the data bit stored in said data bit storage cell matches a reference data bit during a read cycle for said data bit storage cell.

20. For use with a communication system in which a data packet is to be multicast to a plurality of recipients, a method of buffering and controllably supplying said data packet for delivery to multiple ones of a plurality of output ports associated with said recipients comprising the steps of:

(a) storing said data packet to be multicast in only a single data packet storage location of a data packet buffer;

(b) storing, in a content-addressable memory, a plurality of respectively different address pointer words, containing respectively different first fields, associated with multicasting of said data packet to multiple ones of said plurality of output ports, and a common address field that identifies said single data packet storage location of said packet buffer in which said data packet to be multicast is stored;

(c) coupling respectively different keys to said respectively different first fields of said respectively different address pointer words stored in said content addressable memory, to read out contents of said common address field for application to said packet buffer, and thereby cause said data packet to be read out from said single data packet storage location of said packet buffer and multicast to said multiple ones of said plurality of output ports; and

(d) in the course of reading out said contents of said common address field for application to said packet buffer in step (c), coupling said contents of said common address field to address fields of all of the address pointer words stored in said content addressable memory, to determine whether said data packet has been multicast in accordance with each address pointer word stored in said content addressable memory.

21. An output port centric digital data management architecture for a high speed packet switch comprising a content addressable memory which stores address information for controlling multiple accesses to the same data packet stored in a single memory address of a data packet output buffer, to selectively read out therefrom said same data packet to a plurality of ports of the switch, said content addressable memory being configured to store respectively different buffer address pointer words that identify said same data packet to be delivered to selected ones of said plurality of switch output ports, and point to the address of said single storage location of said packet buffer.

22. An output port centric digital data management architecture according to claim 21, wherein a respective address pointer word of said content addressable memory contains a first field that identifies said same data packet, and a companion address field that points to the address of said single storage location of said data packet output buffer, and wherein said content addressable memory is operative, during a first portion of a search thereof, to couple a packet request key to first fields of all address pointer words stored therein, and to cause information associated with a matching first field to access said matching first field's companion address field, said accessed companion address field being employed during a second portion of said search to read out said data packet from said single storage location of said packet output buffer, and to also be simultaneously coupled to address fields of all the address pointer words stored in said content addressable memory, in response to which said content addressable memory outputs a signal indicating whether the accessed address field is contained in another address pointer word stored therein, and thereby whether the address of said single output packet buffer storage location is available to store a new packet.

23. A content-addressable memory having a plurality of storage regions that store respectively different address pointer words, a respective storage region containing:

a first plurality of content addressable memory cells, the contents of which are associated with a first field of a respective address pointer word that identifies data to be accessed from a storage location in a memory; and

a second plurality of content addressable memory cells, the contents of which are associated with a second field of said respective address pointer word that identifies the address of said storage location in said memory.

24. A content addressable memory according to claim 23, wherein respectively different address pointer words stored in multiple ones of said plurality of storage regions of said content addressable memory contain respectively different first fields associated with respectively different ones of multiple instances of accessing said data from said storage location in said memory, and a common second field that identifies the address of said storage location in said memory for each of said multiple instances of accessing said data from said storage location in said memory.

25. A content addressable memory according to claim 24, wherein each of said first plurality of content addressable memory cells is configured to compare contents stored therein with a data access key associated with data to be accessed from said storage location in said memory, and to selectively read out contents of said second plurality of content addressable memory cells to address said storage location in said memory, in accordance with whether or not there is a match between contents stored in said first plurality of content addressable memory cells and said data access key.

26. A content addressable memory according to claim 25, wherein each of said plurality of storage regions is further configured to compare contents stored therein with said read out contents of said second plurality of content addressable memory cells, and to output a signal indicating whether or not said storage location of said memory is available for storage of new data, in accordance with whether or not another of said plurality of storage regions contains said common second field of said respective address pointer word that identifies said address of said storage location in said memory.

27. A content addressable memory according to claim 23, wherein a respective one of said second plurality of content addressable memory cells comprises a data bit storage cell having a data input through which a data bit is written into said data bit storage cell, a data output through which a data bit is read out of said data bit storage cell, and an address input through which said data bit storage cell is selectively accessed, and a data bit comparator coupled to said data bit storage cell and being configured to determine whether the data bit stored in said data bit storage cell matches a reference data bit during a read cycle for said data bit storage cell.

28. A content-addressable memory comprising an array of storage regions that store multibit words, each storage region being formed of a first plurality of content addressable memory cells, the contents of which are associated with a first field of a respective multibit word, and a second plurality of content addressable memory cells, the contents of which are associated with a second field of said respective multibit word, and wherein respectively different words stored in multiple ones of said plurality of storage regions of said content addressable memory contain respectively different first fields, and a common second field.

29. A content addressable memory according to claim 28, wherein said first plurality of content addressable memory cells of a respective storage region is configured to compare contents stored therein with a key supplied thereto, and to selectively read out contents of said second plurality of content addressable memory cells of said respective storage region in accordance with whether or not there is a match between contents of said first plurality of content addressable memory cells and said key.

30. A content addressable memory according to claim 29, wherein each of said plurality of storage regions is further configured to compare contents stored therein with said read out contents of said second plurality of content addressable memory cells to determine whether any other of said plurality of storage regions contains said common second field.

31. A content addressable memory according to claim 28, wherein a respective one of said second plurality of content addressable memory cells comprises a data bit storage cell having a data input through which a data bit is written into said data bit storage cell, a data output through which a data bit is read out of said data bit storage cell, and an address input through which said data bit storage cell is selectively accessed, and a data bit comparator coupled to said data bit storage cell and being configured to determine whether the data bit stored in said data bit storage cell matches a reference data bit during a read cycle for said data bit storage cell.